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Glenn H. Chapman and Nick Pfeiffer
Simon Fraser University,
School of Engineering Science,
Burnaby, B.C., Canada

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Glenn H. Chapman(1), Nick Pfeiffer(2)

1. Simon Fraser University, School of Engineering Science, 8888 University Dr., Burnaby, B.C., Canada V5A 1S6, Tel: (604) 291-3814, Fax (604) 291-4951, glennc@cs.sfu.ca, http://www.ensc.sfu.ca/ensc/people/faculty/chapman/
2. Simon Fraser University, School of Engineering Science, 8888 University Dr., Burnaby, B.C., Canada V5A 1S6, Tel: (604) 826-3461, pfeiffer@uniserve.com

Abstract

Using orbital vacuum for enhanced semiconductor fabrication was pioneered in the Wake Shield project which produced ultra-high vacuums for epitaxial growth of high quality GaAs like materials. A proposed alternative uses the native Low Earth Orbit vacuum levels to achieve the silicon microfabrication processes needed for manufacturing silicon microchips. Space microfabrication combines many processes that are easier to achieve in LEO, potentially producing a flexible range of Microchips (high value per mass products). However standard terrestrial fabrication techniques are difficult to transfer into the microgravity and vacuum environment of space. They are optimized for using in-situ resources: water, power, air pressure and gravity that are plentiful on Earth. An alternative microfabrication process has been developed using the native vacuum environment which could replace wet terrestrial based microfabrication, with significant savings in equipment size, mass and consumables, while reducing cycle time. Computer models have been developed which compare the standard Earth-based process consumables, power and fabrication time with space-oriented processes resulting in a process flow that is optimized for orbital facilities. ISS based microfabrication testing is possible before developing an integrated orbital microchip facility: FabSat .- a synergistic orbital-based system for microfabrication capable of building and delivering commercially marketable microfabricated structures and devices.

Introduction

Low Earth Orbit has two clear environmental aspects not easily obtained on the surface that offer the potential for manufacturing: microgravity and an excellent native vacuum. Much of current space based commercial manufacturing research has focused on microgravity-based products. However while many potential applications have been identified the problem has been finding a material with a large enough value per unit mass and high enough demand for large scale commercial applications.

The alternative advantage of LEO is its native vacuum of $<10^{-8}$ torr. One of the largest users of such a high vacuum is semiconductor manufacturing processes. Using orbital vacuum for enhanced semiconductor fabrication was pioneered in the Wake Shield project[1,2,3,4]. Wakes shield focused on enhancing that native vacuum to still higher ultra-high vacuum levels which are needed for epitaxial growth of high quality III-V materials (GaAs like semiconductors).

A different approach is to consider processes that can directly use those LEO base vacuums levels. This suggests that microchip manufacturing, currently the predominant customer for high vacuum, should be investigated as a space-based industry. This paper looks at a comparison of the requirements for on-orbit semiconductor fabrication of sensors and microchips and those that have been used in the existing Wake Shield program. A feasibility study for semiconductor fabrication in low to medium earth orbit was recently completed that proposes using the International Space Station as a development test bed[5]. This study extended the concept of orbital microfabrication to include all common processes used to produce commercial silicon semiconductor microchips. The key advantage of this integrated, new approach is the use of the native environment found in LEO to provide process vacuum and cleanliness without further environment modification. This paper also summarizes those results.

Why Consider Space Microchip Manufacturing?

To succeed, commercial space manufacturing must create products which have a very high value per unit mass, yet still have a large demand, and for which the space environment provides an important manufacturing advantage. The semiconductor industry is the world's largest manufacturer, producing $180 billion in products and growing at 10-30% annually. The microchips fabricated are very high value, low mass devices ($20,000 - $1,000,000 / kg depending on type). The key to microchip manufacturing is microfabrication, the practice of modifying, growing or depositing thin layers of materials, typically on semiconductor substrates, and patterning those films into precise structures. The repeated application of these processes creates devices ranging from simple solar cells and sensors to complex microchips. What makes this technology important for application in space is the fact that many of the microfabrication deposition and etching processes require base vacuum levels ~10^{-7} torr, above that of low Earth orbit (LEO). This paper suggests that the free vacuum in orbit, with pressures <10^{-8} torr, makes it an ideal place for many such microchip processes

For microfabrication there is another very important advantage of LEO manufacturing: the ultra clean environment of the native vacuum of space. Starting with that base environment introduces less contamination than even the best terrestrial cleanrooms, as shown in Figure 1. Controlling contamination in the microfabrication facilities is extremely important of successful fabrication with a good rate of success for modern chips with their very small minimum geometry (<0.18 micron) of circuit structures. Current microchip manufacturing employs class 1 cleanrooms, where there is less than one particle of 0.5 micron size per cubic foot of air. Based on measured contamination levels the LEO facility has a native level of better than a class 0.001 cleanroom. This is superior to even the best facilities on earth. Furthermore, unlike earth based microfabrication facilities, there is no source of additional contamination in the local environment. Hence the problem becomes one of maintaining this clean condition and not introducing problem materials, rather then of keeping out the local contaminates as on the ground.

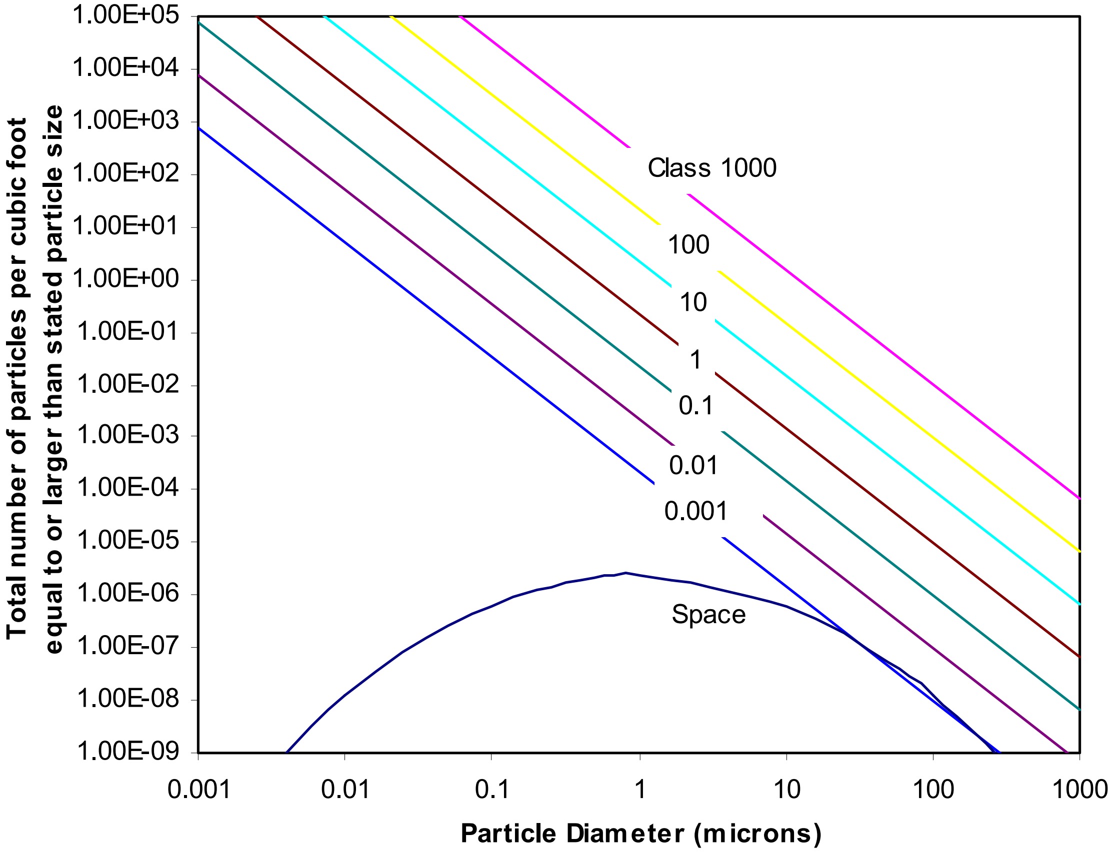


Figure 0.1 – Cleanliness of Space and Cleanroom Environments

Wake Shield's single process orbital microfabrication targets the creation of substrates for later manufacturing on earth. By comparison, space microchip fabrication does have a significantly more complex process flow. Even the most uncomplicated semiconductor devices require the combination of many microfabrication steps, especially those of thin layer deposition, photolithography which then defines the layer into the desired pattern, and etching, which shapes the material creating microstructures. Without this complete set of processes not even the simplest sensors, let alone complex microchips, could be built. Furthermore researchers find that patterned test structures are often necessary to measure important deposited material parameters, such as film thickness uniformity, resistivity, dielectric strength, adhesion and conformality. This is especially true in the case of metal films where optical techniques cannot be used. The key to careful control of microfabrication processes is to create and measure such structures soon after deposition. Thus for both research into potential orbital microchip manufacturing and for the fabrication of useful structures multiple microfabrication processes must be performed in space.

Space-based microchip manufacturing has been suggested previously by Chapman[6], but that preliminary study indicated research was needed in several areas. This has been accomplished in a much more detailed study[5], parts of which will be summarized in this paper. Standard terrestrial fabrication techniques are difficult to transfer into the microgravity and vacuum environment of LEO. They are optimized to make use of in-situ resources like water, power, air pressure and gravity that are plentiful on Earth. Yet, with the right choice of processes, the advantage of native vacuum greatly reduces the contamination introduced at each layer, and thus significantly cuts the number of microfabrication process steps. At the same time it also decreases fabrication equipment complexity, mass and power requirements, and production cycle time. The long term goal of this study is towards the investigation of an integrated orbital microchip facility, which we call FabSat.- a synergistic orbital-based system for microfabrication capable of building and delivering commercially marketable microfabricated structures.

First let us compare the relative advantages and problems of the two orbital based semiconductor fabrication concepts, Wake Shield and the FabSat concept of full microfabrication.

Comparison of Wake Shield and Orbital Microfabricaiion requirements

Wake Shield and orbital microfabrication each have their own strengths and weaknesses.

(1) Wake Shield focused on one process, epitaxial growth: that is the deposition of a high quality crystalline layer on a substrate. This is done because it is an expensive process and hard to accomplish on earth. However having a single process like epitaxial growth means that the end product has a limited application. They are the starting points for fabrication of other devices in the microchip processing area. By comparison a general micro-fabrication facility (FabSat) can produce a much more flexible range of products, and products which can be directly used by end consumers. Most importantly a generalized orbital microfabrication Fabsat facility would be a truly flexible production facility (Silicon Foundry) which could perform a standard multilevel microchip process (e.g. 30 level CMOS) allowing a wide range of devices to be build simply by sending the microchip design to the facility electronically. By having a broader market, FabSat may be easier to develop the business case for full scale production, although, the relative value of the final product is the determining factor in both FabSat and Wake Shield. The Wake Shield program has been able to demonstrate a market for product but faces the difficult problem of timely response to the market, a major problem for most commercial space programs.

Table 1: Comparison of Wake Shield and Orbital Microfabrication (FabSat) Processes

	Wake Shield	**FabSat**
Vacuum Produced	10^{-12} torr	10^{-7} torr
Process	III-V Epitaxy	CMOS
Finished Product	Epi Wafer – starting point for semiconductor fabrication	Wafer with fully functioning semiconductor devices
Market Share of Finished Product	<5%	95%
Vehicle Orientation	±5°	Not critical
Construction Materials	Ultra low pressure metals	Standard
Process Measurement	Critical	Standard

(2) Since Wake Shield was only performing a single process it made maximum use of that by focusing on the creation of the most valuable multilayered depositions structures that could be built without involving photolithographic and etching processes. This essentially limited the Wake Shield to looking at multilayered structures starting with GaAs (called III-V compound semiconductors) and related alloys (AlGaAs/GaAs multistructures)[4]. However while very important the reality is that GaAs related devices only account for less than 5% of the world semiconductor market, where silicon devices are more than 95%.

(3) Orbital microfabrication's flexibility does come at the cost of using many different fabrication processes, and a more complex processes flow. By comparison Wake Shield needs only focus on variations about a single process. However, for FabSat, most processes are repeated several time. Also the pressure levels used for each will have been established in earth based process development.

(4) The Wake Shield's requirement for epitaxial growth is a base vacuum level (typically below 1^{-10} torr) which is much better the native vacuum levels (1^{-8} torr) of Low Earth Orbit. By comparison native LEO pressures are much better than required for most standard fabrication processes (which use 1^{-3} to 1^{-7} torr pressures). This means the task is much easier for the FabSat in that the main focus is one of not contaminating the local environment rather than creating a better environment. Furthermore removing contamination caused by equipment gets exponentially more difficult as pressure requirements are decreased, making maintaining the lower contamination area a much larger task. For example for a considerable time after deployment Wake Shield pressures stayed at 10^{-9} due to the outgassing of water vapor probably originating from water contamination of the device by the space shuttle[3]. The pressure was reduced to 10^{-12} torr in Wake Shield 2, though this was above the expected 10^{-14} torr. This is an excellent pressure but in reality is similar to those of earthly Molecular Beam Epitaxy (MBE) chambers where similar structures are produced on earth. Hence this limited the hoped for gain of much lower pressures from Wake Shield with a corresponding reduction in contamination of the structures. While further work can certainly improve on these pressures it may be at the cost of more complex equipment and systems.

(5) Even to achieve these low pressures, or go lower, inherently the Wake Shield requirements results in much more complex equipment. Furthermore for III-V the type of materials used become important from a contamination point of view. For example molybdenum and tantulum had to be used in the growth volume wherever possible of Wake Shield[2] while the stainless steel had to be kept in the cooler areas. FabSat's more modest pressures allows use of standard vacuum materials like stainless steel.

(6) To achieve the ultra low vacuum pressures the Wake Shield needed to be a free flyer. The design of the Wake Shield craft required important spatial orientation requirements ($\sim +/-5^{o}$) relative to the orbital direction to push the working pressure significantly below the background LEO value behind the shield[3]. Such orientation maintenance is unimportant for Fabsat as the background level is more than sufficient. Indeed many FabSat processes can probably be developed with external experimentation facilities like the ISS.

(7) Robotic handling that does not introduce additional contamination becomes more complex for the Wake Shield. Even measurement of the pressures levels for control requires much more expensive and delicate equipment. By comparison Fabsat microfabrication in space uses processes and equipment which are already developed for those vacuum pressures higher than LEO values. Equipment requirements to maintain those levels are well understood for terrestrial application. Indeed the 1^{-8} torr in space is so good it avoids many contamination problems existing in current earthly facilities. Pressure measurement is straightforward at these levels.

These relative requirements of both Wake Shield and orbital Microfabrication (FabSat) are summarized in Table 1.

To better understand the changes needed in orbital microfabrication relative the existing earth based processes, first we need to outline the standard processes.

Standard Earth-Based Microfabrication Process Flow

The key to understanding space microfabrication is the alteration of several important steps to work better in the space environment. Microfabrication is the practice of modifying, growing or depositing thin layers of materials, typically on semiconductor substrates, and patterning those films into precise structures. What is important is that a limited set of steps are repeated to create the final product. The repeated application of these processes creates devices ranging from simple solar cells and sensors to complex microchips. There are good descriptions of the semiconductor manufacturing process in several references[7,8], but key aspects are summarized here. This section outlines the important issues for space based microfabrication , but a more detailed description is presented elsewhere[5,9].

Starting material for microfabrication is usually a silicon wafer, a flat thin disk or other substrate, typically 150-300 mm in diameter by 0.5-0.6 mm thick. Microfabricated devices are created by the deposition and patterning of typically between 4 and 30 layers of thin films on these substrates On Earth, even with microfabrication occurring in high quality clean rooms, contamination from the local environment and process steps is continuously occurring. Thus the very first process step at any layer is an intensive wet cleaning which involves liquid chemicals and large quantities of highly purified deionized water, 80 kg per cleaning step per wafer in some fabs. While such cleans may be simplified for depositing only a single layer of material, they are needed in any multi-layer process and are critical to the quality of the films deposited. As we will see replacing such wet cleans with vacuum based ones is made possible by the local clean environment.

After the cleaning typically comes a thin film deposition or oxide growth (see Figure 1(A)), processes with are very space compatible. Oxides are grown by exposing the wafer to oxygen or steam in a furnace at about 1100^{o}C for intervals of a few minutes to hours. Metals such as aluminum alloy or other inorganics are deposited via sputtering by bombarding a target material with accelerated argon ions at pressures of a few milli-torr, which “knock off” atoms from the target material and deposit them onto the wafer surface. Because the quality of the deposited film is critically dependent on the absence of any oxygen or contaminants present in the chamber which may interact with the depositing atoms or the surface of the wafer while the film is being formed, the chamber is typically pumped down to at least 10^{-7}torr before operation. Another common process is chemical vapor deposition (CVD), where two typically gaseous chemicals are reacted at low pressures, sometimes augmented by RF plasmas to enhance the reactions. Again required pressures are in the range of a few millitorr, and pump downs to lower pressures are needed to obtain good quality films. Layer thicknesses vary from tens of nanometers to a few microns.

Figure 1(B) shows the next step, where this layer is then patterned using photolithographic definition, where a thin (~1 micron) coating of an organic, light-sensitive material called photoresist is laid down in a gravity-dependent spinning process. A UV image of the desired pattern is then optically projected onto the surface. Figure 1C shows that after developed in a wet solvent bath the resist is left in the unexposed area, while the exposed region has the resist removed, and baked dry. Replacing these wet processes with vacuum based ones is the key to space microfabrication.

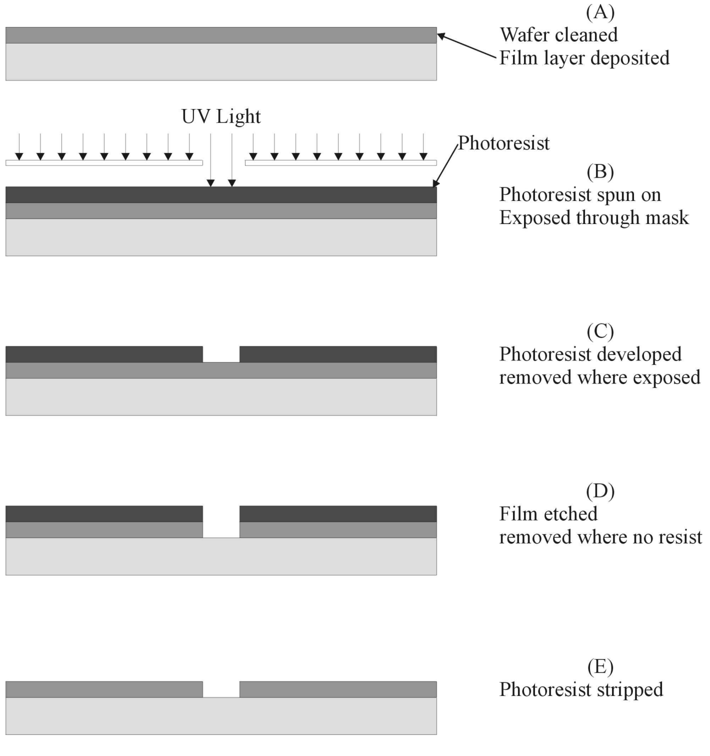


Figure 2: Mains steps in microfabrication process flow for a single level

Figure 1(D) then shows the next step: etching of thin films which removes the pattern areas that are not protected by the resist. While originally wet chemical acid etches were used these have been replaced by dry (vacuum based) processes making these step very space compatible. Dry etching methods all involve good vacuums (starting with 10^{-7} torr) which are then filled with specific gases to a few millitorr pressure for the etching process. Common methods include ion milling (where atoms of argon bombard the film and "knock off" the surface atoms a few at a time), Reactive Ion Etching (RIE) (where specific ions react chemically with the film to remove it), and plasma etching (where an ionized gas reacts chemically with the film). In each case the presence of small contaminants can significantly and adversely affect the uniformity of the etching processes and the quality of the surface left behind.

Finally in Figure 1(E) the photoresist is then stripped, often in an oxygen plasma etcher. However it is very hard to remove all the organics added by the resist, and there is always the danger of introducing other outside contaminants. The cleans at the beginning of each step are needed to remove these contaminants.

This combination of steps - cleans, deposition or growth of a layer, photolithographic definition, etching and resist stripping, is repeated for each layer and pattern to make the final circuit of even the simplest device. Leading edge devices of today require this sequence to be repeated as many as 30 times. It is the use of different patterns and materials at each deposition/definition step that creates the complex circuits of microchips.

When looking space based microfabrication this combination of steps has an important advantage: most deposition and etching processes are already vacuum based. Indeed the process are enhanced by the 10^{-8} torr as many contaminations occur on earth by air leaking into the systems. Indeed the quality of those deposition and etching steps is key to the success of microchip fabrication. It is only the repeated photolithographic wet processes (resist deposition, development and stripping) that are difficult to apply in the vacuum and microgravity environment of space. As already described, the cleanings involve huge quantities of liquids, many of which are difficult to handle in microgravity. The solvents are quite volatile, presenting problems of local contamination to any host space facility. Even the deposition of the photoresist on the wafer presents a problem as it involves gravity and air pressure to work as done on Earth. More importantly the photoresist's constant contamination of the wafers actually removes many of the advantages of the clean vacuum environment. The solution to make microfabrication compatible with the space environment is to switch to a resist that is deposited with a vacuum-based process.

Dry Vacuum-Based Photolithography

To take advantage of the ultra clean environment of the native vacuum of space, which introduces less contamination than even the best terrestrial cleanrooms, the current photoresist process must be changed. This section outlines how vacuum-based resist processes can be substituted, creating significant advantages for space based microfabrication. A more detailed description of the processes involved is given elsewhere[6]. Moreover this is part of the constant trend in microfabrication to switch as many wet processes as possible to dry ones, in spite of the fact that vacuum-based processes are more expensive than wet processes.

While organic-based photoresists are used in microfabrication today there are complications as microfabrication photolithography moves from the current exposures of 248 nm UV to future generations of 193 nm and 150 nm. At those short wavelengths current resists have trouble because the organic materials are destroyed by the UV exposure. Furthermore contamination created by the organics at each photolithographic step creates a constant challenge to maintaining cleanliness at each level. This has lead to studies of inorganic based resists. The problem is that while there are optically sensitive inorganics they often involve materials, such as silver or copper, which destroy transistor operations.

Modern photolithography exposure systems use Eximer lasers as the light source. Rather than a steady UV exposure the wafers are subjected to many 20 nsec. pulses of high powered light, typically 10 mJ/cm^2/pulse. At these power levels significant heat is induced by optical absorption in thin inorganic films creating thermally induced phase changes. Several researchers, including one of the authors (Chapman[10,11]), have been investigating the concepts of inorganic thermal vacuum resist. Typically the films are deposited and developed using vacuum-based processes and hence are referred to as dry resist processes.

One established process available from public literature, developed at Massachusetts Institute of Technology's Lincoln Laboratory, illustrates many of the features of these dry resists[12,13]. This resist consists of a thin, 30 nm film of AlO_x cermets deposited by evaporation or sputtering of aluminum films in the presence of oxygen at $2\text{-}5\times10^{-6}$ torr. The AlO_x is deposited on top of a CVD or sputter-deposited carbon film 1 micron thick. When exposed to Eximer UV laser pulses of 40-100 mJ/cm^2 the AlO_x converts into another aluminum oxide phase known as black aluminum. The films are then developed by Reactive Ion Etching.

All of these inorganic thermal resist processes are dry, that is, involve no liquids and use vacuum-based deposition, development and stripping actions. The full range of film deposition, resist deposition, patterning, etching and stripping can now be done in vacuum-based processes. This means the microstructures are no longer exposed to organic contaminants, and the removal of the multi-stage wet cleans is allowable. A simple ion milling removal of surface material is able to provide a clean on orbit if needed at some points in the space-based process flow. Indeed, it is possible that the high velocity atomic oxygen on the leading edge of an orbital facility could create the source of another cleaning process[14] as oxygen plasmas are extensively used for cleanups in terrestrial microfabs.

The one downside of the AlO_x resist is that it takes a much higher exposure to UV energy, 5-10 times that of organic resists. This is an important problem for Earth-based processing as it significantly slows down the process flows through the exposure systems. Newer, more sensitive inorganic resists are being developed, and there is a strong indication that an industrial trend may emerge favoring these vacuum-based resists.[10]

On Earth there would be concerns that new organics, which are continually introduced into the microfabrication clean room, might contaminate the process. The only way to avoid that is to keep the samples always in a vacuum environment. In space the only significant contaminants would be those imported to the local facility environment. Provided the samples are maintained in vacuum the process as outlined above should be effective in keeping the wafers clean.

Modeling the Advantages of Dry Resist Processing in Space

The FabSat concept evolved from the detailed study of micro-fabrication processing requirements. In a traditional Earth-based semiconductor fabrication facility, a silicon wafer is processed through many steps to deposit, pattern and remove layers of thin films. Each layer forms part of a semiconductor device, with moderately complex devices requiring 20 or more layers. Since most of these layers involves the deposition and etching steps already discussed this processing relies heavily upon the use of vacuum.

The high use vacuum in semiconductor fabrication offers a possible advantage for space-based manufacturing of semiconductor devices. The majority of silicon semiconductor devices are of the CMOS type, accounting for 95% of the world's commercial electronic products. The vacuum requirement to produce CMOS devices is 10^{-7} torr, a level found in low earth orbit. However, while the native vacuum of LEO is sufficient to process CMOS devices, what about other processing parameters such as mass, power, and time?

A recently completed theoretical study [5] examining these issues has shown that with some modification of the standard processes, the mass, power, and time required to process a single silicon wafer compare very favorably with that of Earth-based processing

To obtain the gains from this dry process for a space-based environment this study created a computer model which includes every step of every fabrication process, and the equipment required for each process step. The model uses typical microfabrication process consumables (materials) and equipment for every step. Typical Earth-based equipment, including their vacuum pumps, are included with their volume, mass, process times, power consumed, etc., and space-based equipment models are derived from the Earth-based models taking into account the reductions in mass, volume, and power due to elimination of vacuum systems. .

Items such as liquid/gas flows and solid usages were used to calculate the consumables at each process level. Process times were calculated both on the process times and the time taken to load/unload samples. The model thus assembles complete process flows easily for multi-layer structures. It shows mass of each type of material, process times, and power consumed and its origins. These values were then summarized in charts for each process step. The model's results for larger complicated full CMOS processes are in reasonable agreement with published figures[15] in both power and consumables, especially water.

For the purposes of this paper to compare Earth- and space-based processes using the model a simple three-layer process flow was constructed. This consists of a first level oxidation that was patterned and etched. An aluminum metal layer was deposited, patterned and etched. Next, a top level of CVD oxide was deposited, patterned and etched. This would create a simple test structure that reflects many of the issues connected with more complex devices. The complete study[5] contains a more complex standard 12-level CMOS process, typical of simple commercial chips, was also run as another comparison. Interestingly savings in the main parameters (mass, power and time) is very similar in both the simple 3 level and more complex 12 level. This allowed us with confidence to extrapolate this to a full 20 level process typical many commercial microchips.

For any orbital fabrication facility the important question is how much material mass must be lifted to orbit in order to create the devices. The first consideration is how much material, including the wafer for earthly processes, must be used to build some device. Figure 2 compares the incremental material mass consumption for both wet Earth-based and dry space-based processes. In Earth-based processes almost all the mass consumed is that in the cleaning process, requiring a combined 180 kg for the three levels. In space it is primarily the layer deposition materials and dry resists that are the consumables, with only 0.84 grams used for the structure. This gives a reduction in consumables mass to 0.00047% of the Earth-based process. Since a single 200-mm wafer has a mass of only 40 grams the consumables are small compared to the actual wafer mass. With the more complex, standard 20-level CMOS process, typical of simpler commercial chips, Table 2 shows the actual mass breakdown. The model calculates 1299 kg of material is used for each wafer in an-Earth-based process, almost all of which is water, which is in line with published values[10] for advanced processes. These levels of fluid consumption are unfeasible for space.

The critical process modification needed to achieve the low mass and power requirements was the introduction of a completely dry process flow. In traditional semiconductor processing, fluids, notably water, are used for processes such as cleaning, lithography, and etching. The amount of fluid used is well in excess of 99% of the total mass requirements for the processing .

For space-based processing of the 20-level CMOS devices, the total mass consumed is only 6.9 grams, or about 17% of the wafer original mass, giving a total consumables mass of 0.047 kg. This is only the mass of the materials used, and does not include the containers holding these consumables, and other factors like the masks used in photolithography. Nevertheless this indicates that with the dry resist the process mass requirements for fabricating chips in orbit is very small compared to the mass of the finished chips. Once a processing facility is established the mass of supplies (wafers, processing materials, etc.) will be quite modest on a per wafer basis.

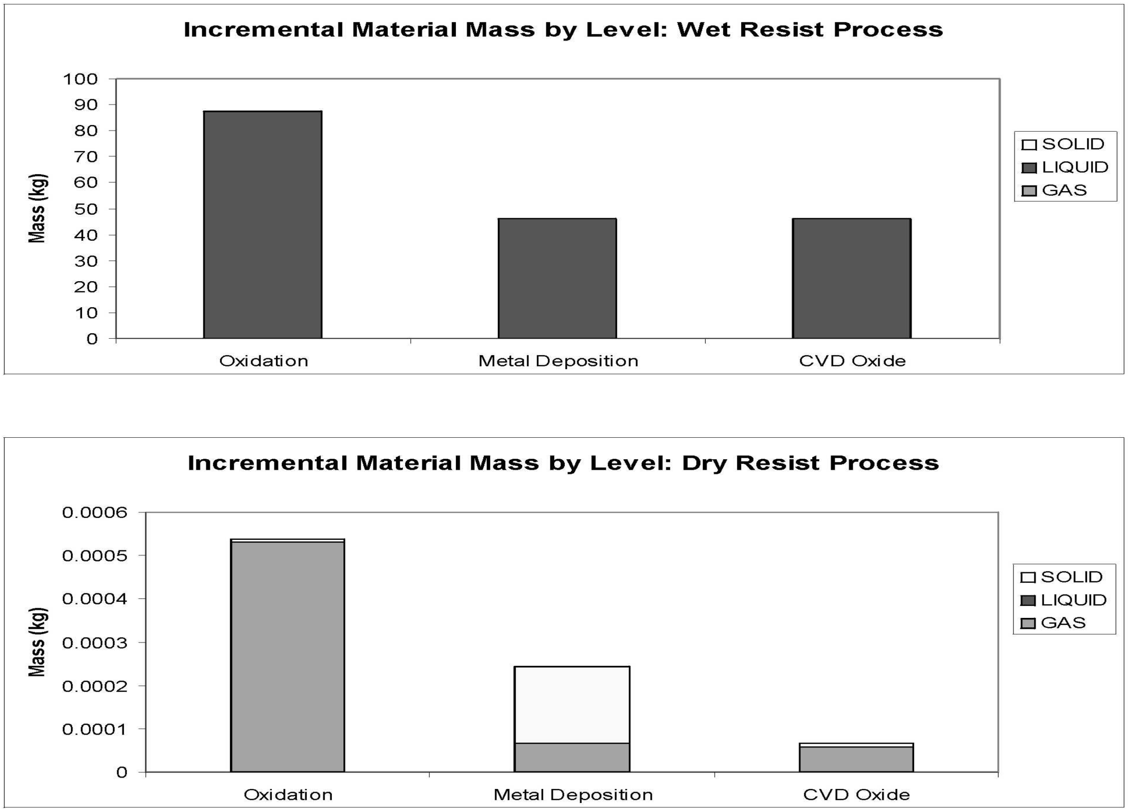


Figure 2 – Incremental Material Mass Consumption for 3-Layer Wet and Dry Resist Processes

Table 2 – Process Material Requirements for a Single, 20 Level, 200 mm Silicon Wafer

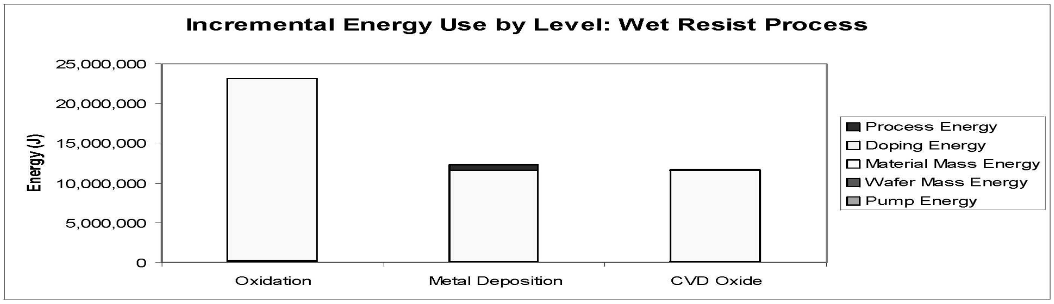
	Earth-Based	FabSat
Gas	0.140 kg	0.0062 kg
Liquid	1298.6 kg	0.0000 kg
Solid	0.0005 kg	0.0007 kg

Figure 3 compares the incremental power usage (energy used per process level) for both wet Earth-based and dry space-based processes. In Earth-based processes almost all the power consumed is in heating the fluids for the cleaning process. The total is a combined 47.2 MJ for the three levels. This power consumption works out to an average of 4.37 kWh per level, which is in agreement with typical terrestrial facilities[10]. In space the process energy to deposit the layer materials and dry resists dominates, totaling 1.6 MJ used to make the structure. This is a power reduction to 3.36% of the Earth-based process, or only 0.15 kWh per level. As Table 3 shows for the more complete 20-level CMOS completed single wafer would consume 3.6 kWh for the average of 4.67 kWh per level[5].

Another important factor is how long the processing cycle time is in space compared to that on Earth. Here, cycle time is defined as the time that elapses from when a wafer begins processing in a fab until the full process sequence is complete and the wafer is ready for final testing, and packaging. In the University of California at Berkeley's Competitive Semiconductor Manufacturing Survey, actual cycle times in modern fabs varied from 1.2 to 3.6 days per masking level[11]. Given the current technology of some twenty to thirty mask levels per wafer, a wafer can spend from 3 weeks to three months in the production line. Table 3 compares the process time used for both wet Earth-based and dry space-based processes. In the Earth-based process flow much of the time is consumed in cleaning and thermal processes connected with depositing the photoresist films, taking a combined 108 hours for the 20 level CMOS.. In space it is the layer deposition of materials and dry resists that dominates, taking only 47.5 hours to build the same structure. This gives a time reduction to 45% of the Earth-based process. For the more less complex 3-layer example process the reduction was larger at 37.5% of the Earth-based processes (because the steps were simpler). Simply stated, chips in space can be produced faster than on Earth

Table 3 – Processing Requirements for a Single, 20 Level, 200 mm Silicon Wafer

	Earth-Based	FabSat
Consumable Mass	1300 kg	0.0069 kg
Processing Power	94 kW-h	3.6 kW-h
Processing Time	105 hours	47.5 hours



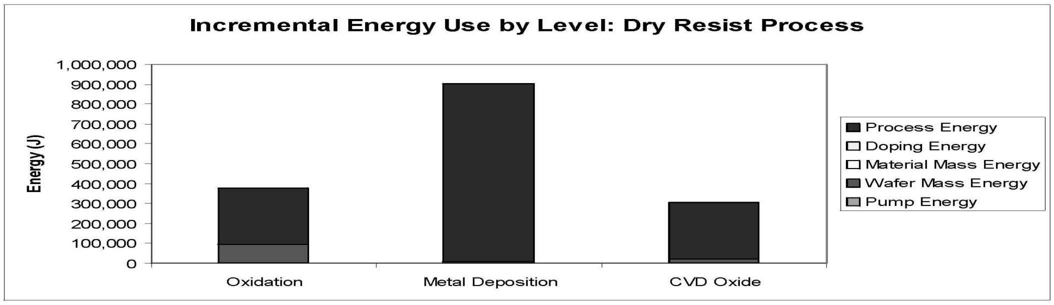


Figure 3 – Incremental Power Use for 3-Layer Wet and Dry Resist Processes

The important result of the material mass and power savings is that a dry resist process changes space-based microfabrication of multi-layer structures from a very expensive process that is nearly impossible to accomplish to one that is possible for both experimental and production purposes. The shorter cycle time enables more effective capital utilization, since that for an equivalent set of equipment the number of wafers processed per hour is increased by about 2.2 times. It is the synergistic savings that comes from the choice of fully vacuum-based processes that make this possible. One trend helping the potential for space-based processing is that Earth-based microfabs are targeting process changes focused on reducing their water and power consumption levels[10]. Another is the push to shorter wavelengths in conventional terrestrial exposure systems may be very difficult with the organic resists, but much easier with the inorganic ones. All of this is driving the Earth-based microfabs to adopt processes similar to the vacuum-based processes outlined here for space usage. These shifts in terrestrial fabrication are more costly to terrestrial fabs, and make space an increasingly attractive alternative over time.

Technical feasibility of FabSat

The important question is: has this mass and power reduction made an orbital microfabrication facility, a FabSat, a technically possible? FabSat, the largest mass reduction comes from the elimination of wet processes, particularly cleaning. The power savings come from the reduction of mass to be heated during processing and is due to elimination of liquid processes. The decrease in processing time is due to many factors: the elimination of wet processes, the adoption of single wafer (parallel) processing in place of batch processing, the use of native vacuum for processing, and the improved cleanliness of the space environment in LEO.

The use of a completely dry process flow does not appear to be feasible in Earth-based fabrication facilities as any contamination of the wafer's surface from the ambient processing environment would prove difficult to remove with dry cleaning processes. However, the completely dry CMOS process flow appears to be well suited for a space-based processing facility that is open to the native LEO vacuum environment.

One important point is that FabSat is not tied to producing only one design. Once a standard process is established different microchips can be manufactured simply by communicating the design (mask descriptions) to the facility. The masks would be produced and wafers run with that set in the standard process. Hence FabSat offers a flexible product output from a standard facility. The supplies used are independent of the microchip design for a given process (e.g. 20 level CMOS) and most designs use such a standard process (specialize chips like memory do use specialized processes).

Table 4 summarizes from the report[5] the requirements for an independent FabSat. The total mass per completed wafer is comprised of the consumable mass, the wafer mass, and the mass of the masks used to pattern the wafer. For a FabSat producing 5000 ASIC wafers per month (20 levels, 250 wafers per mask set), the total product mass requirement per month is 255 kg and the power consumption is 18,000 kWh per month or 600 kWh per day.(achievable solar power levels) Such a FabSat would have a finished product value ranging from $5 to $25 million per month depending on the devices produced. These seem reasonable achievable mass and power requirements for an independent orbital facility. The issue of equipment requirements is also covered in the report[5]. The economic feasibility of FabSat is still under study

Table 4 – Monthly Mass and Power Requirements for 5000 Wafers per Month

	FabSat
Consumable Mass	34 kg
Wafer Mass	184 kg
Mask Mass	37 kg
System Power	18,000 kWh

ISS Based Verification of Space-Based Microfabrication

While the computer models provide interesting results, it is important that process flow and equipment first be verified on Earth. The individual processes can be tested in conventional vacuum chambers used for space vehicles. Testing of the complete process flow and equipment is possible using the largest space environmental satellite testing chambers. These tests would verify such equipment questions as proper chamber design, material flows needed during deposition, and power usage. Once such ground-based tests have verified the equipment operations, including the robotic operations, tests can proceed on space-based facilities. One point to note is that since much current microfab processing is also vacuum-based the robotics for automatic wafer handling in a vacuum are well established.

An ISS-based microfab process prototyping facility should be established. Such a facility would be able to build simple devices such as sensors and transistor circuits to verify the end-to-end process flow in orbit. Fabricating several potential specialized sensor devices offers advantages in measuring the space environment around the ISS because the sensors are never exposed to the Earth atmosphere. Such an ISS test facility could produce these and a wide variety of other useful products very rapidly using only a small number of wafers. Just as with the more complete FabSat the designs could be submitted electronically (uplinked) from Earth, and the finished products either used on the Station or returned to Earth on the Shuttle or other return vehicle. More importantly, this approach would test all the processes needed for building a space-based microfab facility capable of producing commercially useful microfab products.

Conclusions

This paper has explored the technical feasibility of orbital microchip fabrication. Compared to the Wake Shield project such a FabSat has greater flexibility in products and does not need to enhance the LEO vacuum level. It does require a more complex process flow to gain that flexibility. The critical production factors of mass, power, and time have been evaluated and produce substantial saving over Earth-based processes. The high value of the end product (fabricated wafers), coupled with the rising costs of Earth-based fabrication, and offers the possibility of a competitive business case for manufacturing microchips in orbit.

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